



Serial ATA Supplemental Design Guide

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| Supplement ID | 004 |
| Applicable Spec. | 1.0 Gold |

Submission info

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| Name | Company | Date |
| Knut Grimsrud | Intel | 1/8/02 |

Description of design guidance

The Serial ATA Phy parameters defined in the specification are specific to the cabled configuration defined in the spec. Because signal losses through a backplane interconnect are substantially different from those of the cabled configuration defined, designers must be aware that the Phy parameters defined in the specification may not be suitable for a robust backplane implementation.

Supplemental Information

Implementations that utilize an interconnect different from that defined in the Serial ATA specification (such as backplanes) must account for the losses [and signal reflections](#) of that interconnect and compensate accordingly in the host controller transceivers. This may require host controllers that interface with backplane interconnects to have higher transmit amplitudes and greater receiver sensitivities (or other compensating behavior). The burden of such compensation lies on the host controller and no accommodation by devices shall be required or assumed.

Disposition log

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| 1/8/2002 | Submitted for review |
| 1/9/2002 | Inserted clause "signal reflections" as part of describing the PCB interconnect losses |

Technical input submitted to the Serial ATA working group is subject to the terms of the Serial ATA participant's agreement (contributor's agreement).